# Lab 3 Structural Report

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing “yes” at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? Yes

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: \_\_\_\_

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Date Completed: 05-21-2020  
Time Spent: Reviewing Digital Design Material: 1h  
 Design/Preparation Work: 1h  
 VHDL Coding & Debugging: 8h

## Structural Overview

100%

The code runs fine and produces correct value for the output. As ALU can perform one operation at once, so I modified my FSMD. Then I made the control word table for this FSMD and implemented it to the code. Satisfied with the work.

## Lab 3 FSMD & Control Word Table



|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| State | RegFile | | | | | | ALU | Shifter | Selector | OutReg | | Three State Buff | Done |
| Rst | R\_Addr1 | R\_en | R\_Addr2 | W\_en | W\_Addr | Sel | Sel | Sel | Rst | Ld | Oe |
| Initial | 0 | 000 | 0 | 000 | 0 | 000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Calc A (t2) | 0 | 100 | 1 | 100 | 1 | 101 | 1 | x | 1 | 0 | 0 | 0 | 0 |
| Calc B (at2) | 0 | 001 | 1 | 101 | 1 | 101 | 1 | x | 1 | 0 | 0 | 0 | 0 |
| Calc C (1/2at2) | 0 | 000 | 1 | 101 | 1 | 101 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Calc D (v0t) | 0 | 010 | 1 | 100 | 1 | 110 | 1 | x | 1 | 0 | 0 | 0 | 0 |
| Calc E  (1/2at2 + v0t) | 0 | 101 | 1 | 110 | 1 | 101 | 0 | x | 1 | 0 | 0 | 0 | 0 |
| Calc F (1/2at2 + v0t + x0) | 0 | 101 | 1 | 011 | 0 | xxx | 0 | x | 1 | 0 | 1 | 0 | 0 |
| Result | x | x | x | x | x | x | x | x | x | x | x | 1 | 1 |

## Lab 3 Minimum Clock Cycle

Minimum clock cycle: 37 ns

Longest clock-to-clock path

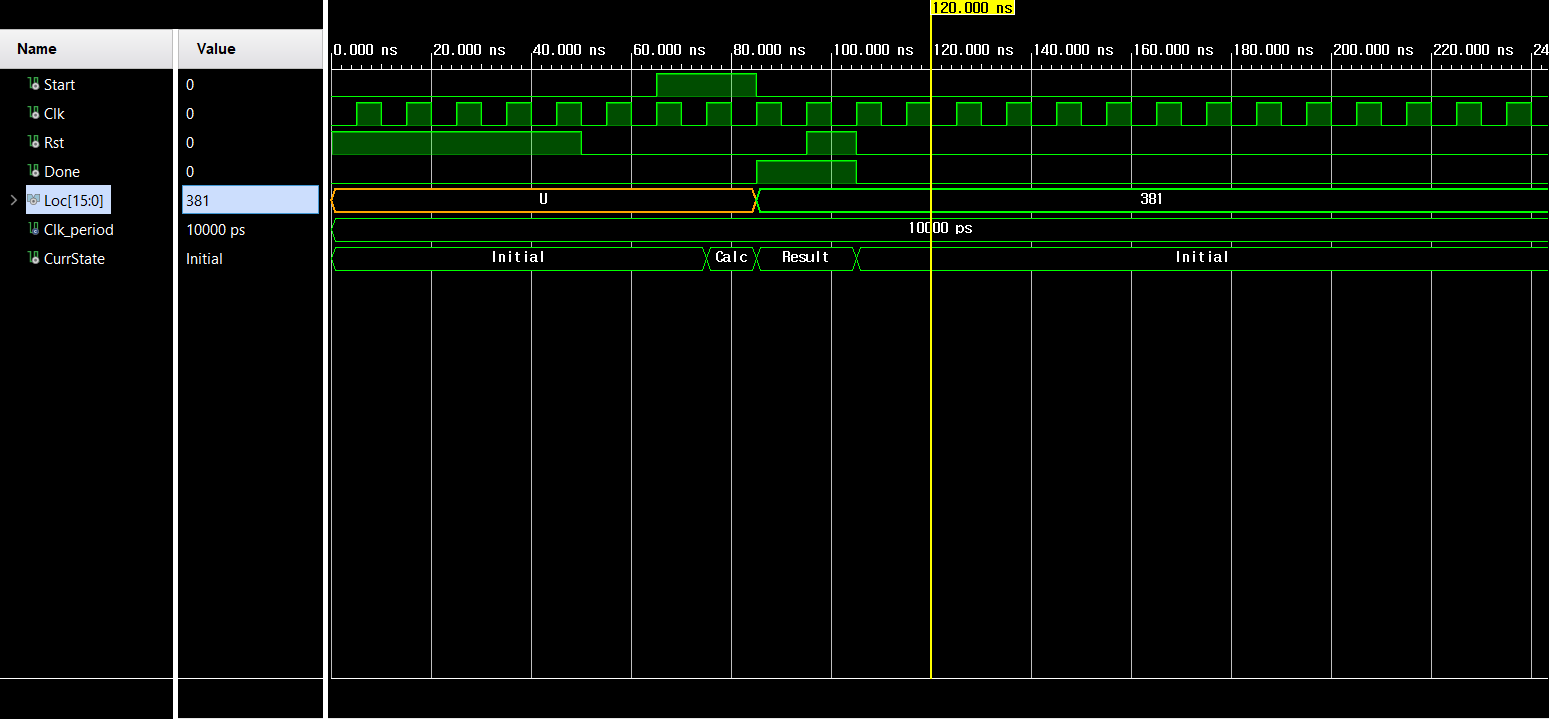
4 ns (StateReg) + 11ns (CombLogic) + 6 ns (RegFile) + 12 ns (ALU) + 3 ns (Selector) + 1 ns (OutReg setup time) = 37 ns

## Lab 3 Structural Simulation Graph



## Lab 3 Structural and Behavioral Simulation Graph Comparisons

Behavioral



For behavioral, I kept the final value in Loc when it is not reset. However, in structural, Loc is always in high impedance if currstate is not Result. Calculation state has been more separated from behavioral to structural. Clock cycle has been specifically set for structural, too. Since the tristate buffer is used in structural, Loc has Z value instead of U, which is different from behavioral.